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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,417	06/15/2001	Eric G. Chambers	5500-67700	8413

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EXAMINER	
ABRAHAM, ESAW T	
ART UNIT	**PAPER NUMBER**
2133	3

DATE MAILED: 03/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,417	CHAMBERS ET AL.	
	Examiner	Art Unit	
	Esaw T Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/01/22/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims **1 to 15** are presented for examination.

Information Disclosure Statement

2. The examiner has been considered the references listed in the information disclosure statement submitted on 01/22/02 (see attached PTO-1449).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. For example: the phrase "said erroneous data" in claim 3, line 27 and in claim 8, line 17 is not known to independent claims 1 and 6.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims **1-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzales et al. (U.S. PN: 6,101,614).

As per claims **1 and 11,** Gonzales et al. teach or disclose method and apparatus for automatically scrubbing ECC errors in memory upon detecting correctable errors in data read from memory through the use of a write back path coupled between the outputs of the read and write data buffers of a memory controller (see abstract and col. 3 last paragraph). Further, Gonzales et al. teach a memory controller comprising a memory interface to read data from an address in memory indicated by a memory read request, an error checking and correcting (ECC) logic coupled to receive the data read from the address in memory whereby the ECC is being configured to detect whether the data has a correctable error and to issue an error signal and correct the correctable error to generate corrected data if the data has a correctable error, a control logic (control unit) coupled to receive the error signal from the ECC whereby the control logic is being configured to tag the memory read request in response to the error signal to indicate that the data has the correctable error, and write the corrected data back to the address in memory indicated by the tagged memory read request (see col. 8, lines 37-49 claim 8). Furthermore, Gonzales et al. teach that the control logic further configured to issue a scrub command to establish a write back path to write the corrected data back to the address in memory indicated by the tagged memory read request (see claim 10). Although, Gonzales et al. **do not explicitly teach** or is silent to teach a storage unit coupled to the control unit, Gonzales et

al. teach a control logic being configured to tag the memory read request in the request queue (a queue is known to be a sequence of messages or jobs held in a **storage** awaiting for transmission or processing) in response to the error signal to indicate that the data has an error, which Gonzales et al. is basically identifying or indicating an error and configuring to store an erroneous data. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to store an address or an erroneous data in a memory sub system to indicate an error. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because a storage is a functional unit into which data can be entered, in which they can be retained, and from which they can be retrieved and further storages (buffers, registers etc....) are well known components or features of any memory controller.

As per claims **2, 7 and 12,** Gonzales et al. all the subject matter claimed in claims 1, 6 and 11 including Gonzales et al. teach that an error checking and correcting (ECC) logic coupled to receive the data read from the address in memory whereby the ECC is being configured to detect whether the data has a correctable error and to issue an error signal and correct the correctable error to generate corrected data if the data has a correctable error, a control logic (control unit) coupled to receive the error signal from the ECC whereby the control logic is being configured to tag the memory read request in response to the error signal to indicate that the data has the correctable error, and write the corrected data back to the address in memory indicated by the tagged memory read request (see col. 8, lines 37-49 claim 8).

As per claims **3, 8 and 13,** Gonzales et al. all the subject matter claimed in claims 1, 6 and 12 including Gonzales et al. teach that a memory controller comprising a memory interface to read data from an address in memory indicated by a memory read request (see claim 8).

As per claims **4, 5, 9, 10, 14 and 15,** Gonzales et al. all the subject matter claimed in claims 1, 6 and 11 including Gonzales et al. teach in conventional software-based scrubbing process, the detection of a correctable error in data being read from memory causes microcode to save the logical address of the errored memory location and generate a system call to an interrupt (inhibit) routine and the invoked interrupt routine then uses the logical address to calculate the physical address of the memory location and to re-read the data from the specified memory location and as the data is again read from memory, it is input to an ECC checking and correcting circuit to correct the data and further after the data has been corrected, the interrupt service routine issues instructions to the microprocessor to cause the data to be written back to the same location in memory once the data has been placed on the system bus and the appropriate requests are made to the microprocessor (see col. 1, last paragraph).

As per claim **6,** Gonzales et al. all the subject matter claimed in claim 1 including a system comprising a system bus, one or more processors, a memory, a memory controller coupled between a system bus and the memory whereby the memory controller including a request queue to store memory access requests received via a system bus, a memory interface to read data from an address in the memory indicated by a memory read request that is queued in the request queue, an ECC logic coupled to receive the data read from the address in the memory whereby the ECC logic being configured to detect whether the data has a correctable error and to issue an error signal and correct the correctable error to generate corrected data if the data has a

correctable error and a control logic coupled to receive the error signal from the error checking and correcting logic whereby the control logic being configured to tag the memory read request in the request queue in response to the error signal to indicate that the data has the correctable error, and write the corrected data back to the address in the memory indicated by the tagged memory read request before retiring the tagged memory read request from the request queue (see claim 14). Gonzales et al. **do not explicitly teach** or is silent to teach a storage unit coupled to the control unit. **However,** Gonzales teaches a control logic being configured to tag (store an indication) the memory read request in the request queue (a queue is known to be a sequence of messages or jobs held in a storage awaiting for transmission or processing) in response to the error signal to indicate that the data has the correctable error which Gonzales et al's memory read request in request queue is basically tagging or storing an indication in a storage unit. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to store an address or an erroneous data in a memory sub system to indicate an error. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because a storage is a functional unit into which data can be entered, in which they can be retained, and from which they can be retrieved and further storages (buffers, registers etc....) are well known components or features of any memory controller.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,560,725 Longwell et al.

US PN: 6,591,393 Walker et al.

6. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

Guy J. Lamarre
for

Albert DeCady
Primary Examiner